Constrained Partial Response Receivers for High-Speed Links

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***Abstract*—This paper presents an architecture and an optimization framework that uses partial response (PR) equalization for high-speed links. PR equalization is achieved through a combined use of linear transmit equalization and decision feedback equalization (DFE). This technique outperforms full-channel/impulse equalization for a wide range of channels in wireline communication. The constrained PR response equalization technique presented here improves eye openings, reduces the overall bit error rate, and reduces crosstalk impact for a large class of channels while maintaining a simple implementation. The new transceiver architecture proposed is particularly well suited for high-speed multichannel applications due to the mitigated DFE loop timing constraint. In comparison with duobinary equalization, the proposed PR architecture improves the eye height and eye width of the receiver by 28% and 10%, respectively, at 10 Gb/s and by 19% and 7%, respectively, at 15 Gb/s. The performance improvements in comparison to impulse equalization are even larger.**

***Index Terms*—Bit error rate (BER), decision feedback equalization (DFE), minimum mean-squared error (MMSE), partial response (PR), pulse amplitude modulation (2-PAM).**

I. Introduction

THE persistent demand for increasing data throughput in computer desktops and servers has pushed high-speed serial links to the limits of their performance. Channel loss and imperfections in the channel frequency response, due to impedance discontinuities, lead to intersymbol interference (ISI) and limit the overall link throughput. Additionally, crosstalk from neighboring channels cause timing and amplitude errors at higher speeds. All of these nonidealities exacerbate the eye closure at the receiver and adversely affect the bit error rate (BER) of the overall link. Linear equalizers are often used in state-of-the-art high-speed links in order to ensure signal integrity [1]. The most common technique used is pulse amplitude modulation (2-PAM), baseband signaling with full-channel equalization where the combined response of the equalizers and the channel is forced to a single impulse, i.e., zeroing out all ISI components [1]–[4]. More recently, duobinary and 4-PAM equalization techniques have been tried out in high-speed serial links [3], [4]. One of the major goals of this research is to extend the use of the different equalization techniques and demonstrate the potential benefits provided by partial response (PR) channel equalization for future high-speed links.

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The successful use of PR equalization in disk drive channels is well documented [6], [7]. Many of these techniques can be applied to wireline communications as well. For a fixed channel, as the data rate increases, the number of postcursor and precursor ISI components increases. Here, the cursor is defined to be the largest tap in the response. Instead of attempting to equalize all of the precursor and postcursor taps to zero, some controlled amount of ISI, determined by a known target PR, can be allowed to remain in the equalized response [5], [6]. This normally results in a larger eye opening at the receiver. Power supply limitations in practical wireline systems place constraints on the peak transmit power (peak transmit voltage) rather than the average power. Therefore, this constraint should always be used when comparing wireline systems [2]. In this research, a PR equalization and detection framework is developed that equalizes channels to a near-optimal target PR. In other words, the channel is shaped to be sufficiently close to the desired response, while limiting the architecture complexity for a given channel. Practical nonidealities such as impedance discontinuities, crosstalk, and circuits noise are incorporated into the optimization problem. Based on our analysis, an architecture suitable for a variety of channels is proposed that uses a linear equalizer at the transmitter combined with a 1-tap decision feedback equalizer (DFE) at the receiver. This architecture was applied to a class of channels used in high-speed memory applications and showed improved performance when compared with other equalization techniques. Additionally, the new architecture mitigates the tight DFE loop timing issue and relaxes receiver circuit design in terms of speed.

II. Generalized PR Equalizers

In current day high-speed links, signal integrity issues are usually addressed by equalizing the distorted signal. The performance is improved by increasing the number of taps in the transmit finite impulse response (FIR) equalizer or receiver DFE to remove the majority of the ISI [1]. Full-channel transmit equalization (PR_1) to a single impulse can result in a smaller eye opening in comparison with PR equalization when the channel impulse/pulse response has strong ISI components. Fig. 1 shows a typical serial link channel pulse response which is equalized to a general target PR of $[b_1.1.b_2.b_3.b_4]$ (this is the combined response of transmit equalizer and the channel), where the b_i's are the tap values calculated by an optimization algorithm, as will be explained in Section IV. As shown later in Fig. 2, this response is fairly typical of measured channels. Forcing all of the ISI taps to zero normally results in a smaller eye opening when the channel pulse response is similar in shape to that shown in Fig. 1. Not surprisingly, equalizing the pulse response to a target PR closer to the channel pulse response,

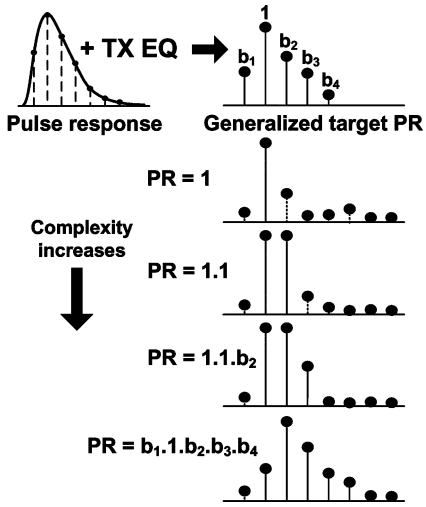

Fig. 1. Generalized and constrained PR equalization technique.

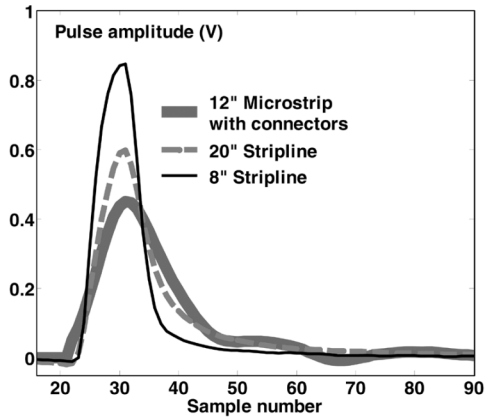

Fig. 2. Measured stripline and microstripline channel pulse responses.

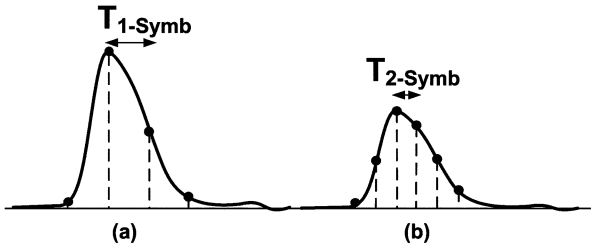

Fig. 3. (a) General impulse response at $T_{1-\mathrm{Symb}}$ and (b) at $T_{2-\mathrm{Symb}}$.

i.e., using a matched filter, results in a larger eye opening at the receiver. Fig. 1 also shows different PRs that can be used as the target response during equalization. Here, PR_1 is the full channel equalization, $\mathrm{PR}_{1.1}$ is duobinary equalization, $\mathrm{PR}_{1.1.b2}$ is the proposed PR equalization and $\mathrm{PR}_{b1.1.b2.b3.b4}$ is the generalized target PR that might be required for higher speeds. In PR equalization, a predetermined amount of ISI is allowed to remain which can be optimally detected by a maximum-likelihood sequence detector (MLSD). However, MLSD implementations are too complex and require extremely high power for the speeds required in serial links. We propose a novel link architecture in Section IV for the $\mathrm{PR}_{1.1.b2}$ target, which can be used for a wide range of channels. Fig. 2 shows measured pulse responses for two stripline channels with different lengths and a microstrip channel with connectors commonly used in high-speed links. We note that the measured pulse responses for the various channels look surprisingly similar to the model shown in Fig. 1. Fig. 3(a) and (b) illustrates typical channel pulse responses at two different rates and their corresponding cursor (main tap), precursor, and postcursor taps. The number of precursor and postcursor ISI components are fewer at the lower symbol rate, $1/T_{1-\mathrm{Symb}}$, therefore equalizing all of the ISI taps to zero results in little or no penalty in the eye opening at the receiver. At higher speeds, $1/T_{2-\mathrm{Symb}}$, the number of ISI components increase relatively as shown in the figure and equalizing them to zero reduces the receiver eye opening. PR equalizers alleviate this issue, improve eye opening, and limit noise boost. A new link architecture is required to resolve the controlled ISI and perform detection. It is worthwhile to note that the implementation complexity increases when dealing with a more general PR, hence there is a tradeoff in determining the optimum PR to be used for a particular channel response. Additionally, when the channel is equalized to a nonimpulse PR, both the overall occupied signaling bandwidth and crosstalk are reduced. This is discussed in more detail in Section III.

III. Crosstalk in PR Equalization

In parallel high-speed links, far-end crosstalk (FEXT) is one of the major noise sources at higher frequencies and reduces the signal-to-interference ratio (SIR) [7]. Full-channel transmit equalization (PR_1) is suboptimal at higher speeds, as it has a high-pass frequency response and boosts the crosstalk. Fig. 4 shows the frequency responses of the different PR equalizers when optimized for a given channel with a fixed number of taps. As seen in the figure, PR_1 boosts the higher frequencies the most. We define a figure of merit (FOM), $\mathbf{y}_{\mathrm{Rx-rms}}/\mathbf{y}_{\mathrm{Xt-rms}}$, which is the ratio of rms received signal to the rms crosstalk noise from the adjacent lines (FEXT). This FOM can be used to evaluate PR equalizer performance in high-speed links with respect to crosstalk. In fact, this FOM is the effective $\sqrt{\mathrm{SNR}}$ when crosstalk is the dominant interference and noise term. Table I summarizes the FOMs for the channel model discussed in [7] for different target PR equalizers. Due to the reduced high-frequency boost of the more generalized PR equalizer, they are particularly well suited for link environments where crosstalk problems dominate.

IV. Novel Architecture for Memory Channels

For each of the measured responses shown in Fig. 2, the number of ISI components increase at higher data rates and a target PR of $[1\ 1\ b_{\mathrm{opt}}]$ offers a reasonable match. Here, b_{opt} is the optimum b calculated using the minimum mean-square error (MMSE) optimization algorithm discussed in Section V. For the remainder of this paper, we focus on the $\mathrm{PR}_{1.1.b}$ target. This target is an extension of duobinary $(\mathrm{PR}_{1.1})$ and yet maintains reasonable implementation complexity. Fig. 7 shows the proposed architecture for the $\mathrm{PR}_{1.1.b}$ target. Just as in duobinary, the precoder is a differential precoder, which shapes the channel to $1/(1 \bigoplus D)$ and results in the removal of the prior bit history from the current symbol [8]. The precoder helps to reduce the receiver overhead and makes it possible to decide the received data bit on a symbol-by-symbol basis. Here, $\mathbf{h}$ is the victim

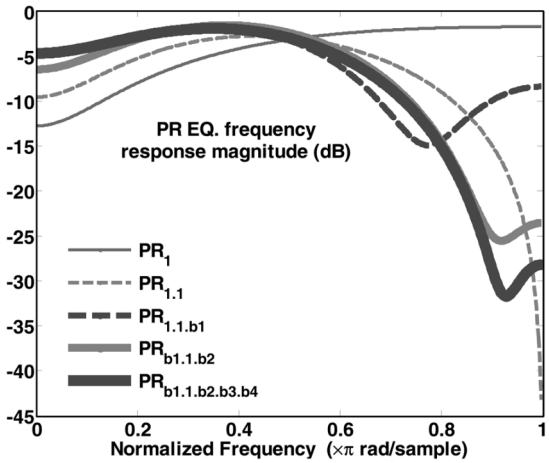

Fig. 4. Frequency response of different target PR equalizers.

TABLE I
CROSSTALK FOM FOR DIFFERENT PR EQUALIZATION TARGETS FOR THE CHANNEL MODEL WITH 30-IN LENGTH AND 20-MIL SEPARATION [7]

PR	*1*	*1.1*	*1.1.b_2*	*b_1.1.b_2*	*b_1.1.b_2.b_3.b_4*
$\frac{y_{Rx-rms}}{y_{Xt-rms}}$	*19*	*28*	*34*	*34*	*39*

channel impulse response and $\mathbf{h}_{\mathrm{CTl}}$, $\forall l\ 2 \le l \le m$, are the aggressor(s) (crosstalk) impulse responses. Pre-emphasis taps on the transmitter side are optimized as explained in Section V. The detector at the receiver includes a duobinary two-level slicer combined with some simple logic, which detects the transmit data at each decision instant [4]. The impact of the known post-cursor tap b_{opt} is removed by using a 1-tap DFE and a post-coder which is identical to the pre-coder shown in the Fig. 7. The post-coder is needed to correctly cancel the post-cursor tap (b_{opt}). Note that the DFE post-cursor tap (b_{opt}) is delayed by two symbol periods, i.e., the DFE loop timing constraint is relaxed by nearly two times in comparison to traditional DFE architectures. In traditional high-speed links, the DFE loop timing is a critical implementation issue as the data rate increases. Loop unrolling, which is required to alleviate this timing problem, results in increased power consumption due to its parallel nature [9]. Our proposed architecture is an alternative solution for high-speed operation in general and to DFE loop unrolling due to the additional delay in the feedback path, which relaxes the loop timing problem normally associated with DFE receivers.

Unfortunately, like other PR equalization schemes, timing recovery here is not as straightforward as full-channel equalization since the incoming symbol is the weighted sum of three consecutive bits and has multiple transitions within each symbol interval. An extended version of the timing recovery techniques developed for duobinary and 4-PAM signaling may be required for improved performance [1], [3]. In this paper, we will primarily focus on channel equalization.

V. MMSE OPTIMIZATION PROBLEM

An MMSE optimization framework for the transmit equalization taps has been developed for generalized PR equalizers where crosstalk noise has also been incorporated into the optimization problem. Here, we focus on the optimization problem

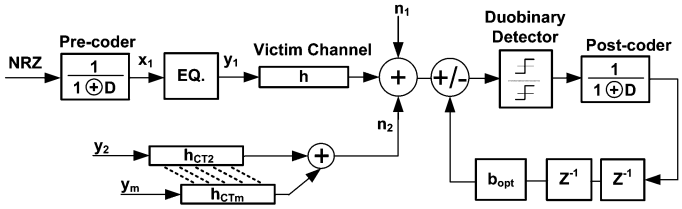

Fig. 5. Stripline and microstrip channel responses.

for the architecture presented in the previous section with a target PR of $[1\ 1\ b]$. More generalized forms of PR have also been analyzed in our optimization framework but, for this discussion, we only focus on $\mathrm{PR}_{1.1.b}$. The set of equations in (1) is used as a basis for the MMSE problem and contains the symbols shown in Fig. 5. Here, x_1 is the random input data stream, y_l is the equalized transmitted data on the parallel lines, n_2 is the sum of the equalized crosstalk noise from adjacent lines at the receiver, s is the ideal target PR for $\mathrm{PR}_{1.1.b}$ response, and n_1 is white thermal noise at the receiver with a power spectral density of σ_{n1}^2. Likewise, h, h_{CTl} and f are the symbol-rate channel impulse response, crosstalk impulse response, and equalizer tap vectors, respectively. Additionally, z, ε, and J are the received equalized symbol, symbol errors, and error power, respectively

$$\begin{aligned}
y_l(k) &= (x_l * f)(k), \quad \forall\, l1 \le l \le m \\
n_2(k) &= \sum_{l=2}^{m} (y_l * h_{\mathrm{CTl}})(k) \\
s(k) &= x_1(k) + x_1(k-1) + bx_1(k-2) \\
z(k) &= (x_1 * f * h)(k) + n_2(k) + n_1(k) \\
\varepsilon(k) &= s(k) - z(k) = x_1(k) + x_1(k-1) + bx_1(k-2) \\
&\quad - (x_1 * f * h)(k) - n_2(k) - n_1(k) \\
J &= E[\varepsilon(k)\varepsilon(k)^*]. \qquad (1)
\end{aligned}$$

The following criteria holds for $\forall i - L \le i \le L$ using the MMSE problem for symbol error power, J, defined above:

$$\frac{\partial J}{\partial f(i)} = 0, \quad \frac{\partial J}{\partial b} = 0 \qquad (2)$$

$$E[(h * x_1)(k-i) + n_2(k-i)]\varepsilon(k)\} = 0. \qquad (3)$$

Equation (3) follows the criteria in (2) with J as defined in (1). Rearranging the above equations leads to the following set of equations for $\forall i - L \le i \le L$ with b_{opt} as the optimum variable tap in the target $\mathrm{PR}_{1.1.b}$ and f_{opt}'s as the optimum pre-emphasis tap values:

$$b_{\mathrm{opt}} = \sum_{p=-L}^{L} f_{\mathrm{opt}}(p) h(2-p) \qquad (4)$$

$$\begin{aligned}
h(-i) + h(1-i) = \sum_{p=-L}^{L} f_{\mathrm{opt}}(p) \\
\times \Bigg[\sum_{m} h(m)h(m-p+i) \\
+ \sum_{l=2}^{m} \sum_{v} h_{\mathrm{CTl}}(v) h_{\mathrm{CTl}}(v-p+i) \\
- h(2-p)h(2-i) \Bigg]. \qquad (5)
\end{aligned}$$

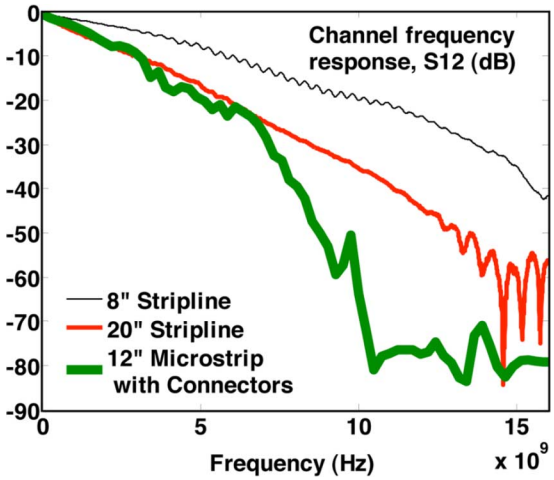

Fig. 6. Microstrip symbol rate pulse response at 10 Gb/s.

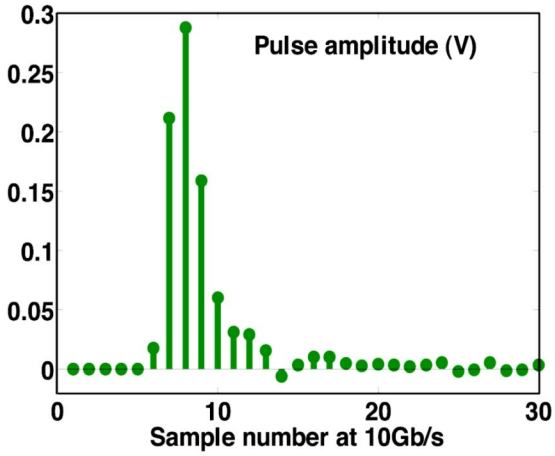

Fig. 7. System link architecture for a PR target of $[1\ 1\ b_{\rm opt}]$.

To provide a closed-form expression for $f_{\rm opt}$, optimized taps vector, (5) can be written in matrix form as

$$f_{\rm opt} = h_v(H + H_{\rm CT} - H_2)^{-1}. \tag{6}$$

The elements of h_v and the square matrices H, $H_{\rm CT}$, and H_2 are defined for $\forall\, i,p$ with $-L \le i,p \le L$ as follows:

$$\begin{aligned} h_v(i) &:= h(-i) + h(1-i) \\ H &:= \left[\sum_m h(m)h(m-p+i)\right]_{pi} \\ H_{\rm CT} &:= \left[\sum_{l=2}^{m}\sum_v h_{\rm CTl}(v)h_{\rm CTl}(v-p+i)\right]_{pi} \\ H_2 &:= [h(2-p)h(2-i)]_{pi}\,. \end{aligned} \tag{7}$$

Likewise, $J_{\min}$ is obtained by replacing the equalizer tap vector (f) and the variable tap value (b) with their optimum values for the J in (1). $J_{\min}$ is often used as a performance comparison metric as explained in Section VI:

$$\begin{aligned} J_{\min} =& 2 + (f_{\rm opt} * h)(f_{opt} * h)' - b_{\rm opt}^2 \\ & - 2\sum_{p=-L}^{L} f_{\rm opt}(p)\,\{h(-p) + h(1-p)\} \\ & + \sum_{l=2}^{m}\{(f_{\rm opt} * h_{\rm CTl})(k) \\ & \qquad \times (f_{\rm opt} * h_{\rm CTl})'(k)\} + \sigma_{n1}^2. \end{aligned} \tag{8}$$

VI. Performance Comparison of PR Equalizers

Here, we discuss the link performance results for the different target PR equalizers. The frequency responses of the measured channels are shown in Fig. 6 which correspond to the pulse responses shown in Fig. 2 earlier. High-level Matlab models were developed for simulating the link behavior for various target PRs at different speeds with the built-in optimizer discussed in the previous section. As discussed in Section II, the choice of the optimum PR depends on the channel pulse response and on the data rate at which the link operates. The minimum symbol error power $J_{\min}$ is a suitable FOM for the comparison of various equalizers and for different target PRs. This parameter is closely correlated to BER of the link, but, unlike BER, $J_{\min}$ can be calculated directly from the MMSE problem as in the previous section, which makes the comparison process much easier than simulating the BER. We use the $J_{\min}$ results as a primary guide to compare the different target PRs and eye width and eye height for the final comparison metrics in this research. As mentioned before, the TX peak voltage is limited to a fixed value for all of the cases presented in this section. The channel used for the simulations is a $12''$ channel with connectors where Fig. 6 shows its frequency response and Fig. 7 shows its pulse response. This channel is an example of commonly used channels in current high-speed links and is used for the simulation results in the current section. In this example, there is very little crosstalk (intentionally by design) and the residual ISI is the dominant factor in the eye closure at the receiver. Fig. 7 is the sampled pulse response of the discussed channel at 10 Gb/s which is a good match for the target PR of $[1\ 1\ b]$. For data rates above 10 Gb/s and for the current channel data, $\rm PR_{1.1.}{\it b}$ performs better than both $\rm PR_1$ and $\rm PR_{1.1}$ equalizations. The value of the optimized parameter, $b_{\rm opt}$, varies with the data rate. Fig. 8 shows $J_{\min}$ values for the different target PRs for the given channel. $J_{\min}$ is calculated for different numbers of TX equalizer taps.

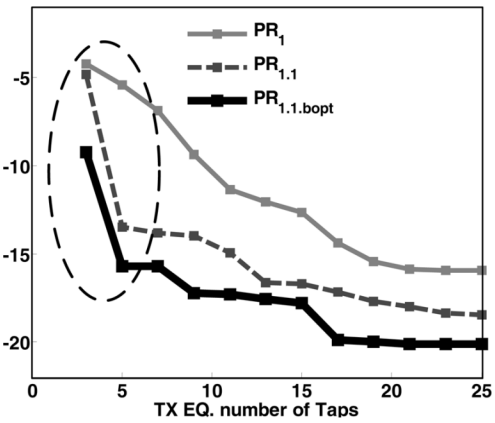

Fig. 8. $J_{\min}$ variation versus number of TX equalization taps and different PRs.

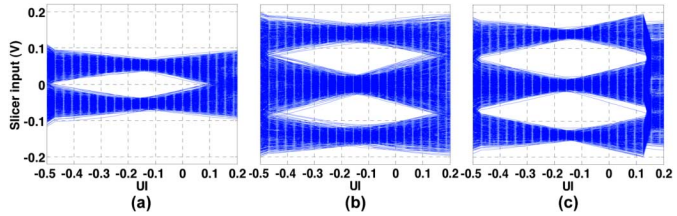

Fig. 9. PR equalizer eye diagram at 10 Gb/s. (a) PR_1. (b) $\mathrm{PR}_{1.1}$. (c) $\mathrm{PR}_{1.1.b}$ with $b_{\mathrm{opt}} = 0.0515$.

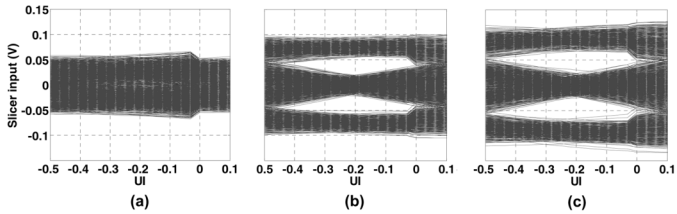

Fig. 10. PR equalizer eye diagram at 15 Gb/s. (a) PR_1. (b) $\mathrm{PR}_{1.1}$. (c) $\mathrm{PR}_{1.1.b}$ with $b_{\mathrm{opt}} = 0.0613$.

Many recently published results on high-speed links use more than three pre-emphasis taps. Fig. 8 highlights the region for a practical number of pre-emphasis taps. The figure shows a reduction in the minimum achievable symbol error power by using the more generalized PR equalizers. The best performance is provided by $\mathrm{PR}_{1.1.b}$ (lowest $J_{\min}$) when compared to PR_1 and $\mathrm{PR}_{1.1}$ equalizations. PR equalizers with a larger number of taps results in lower residual ISI and correspondingly lower $J_{\min}$. As illustrated in the figure, $J_{\min}$ does not improve for tap numbers greater than 15 due to the complete cancellation of ISI. However, the difference in the performance floors are due to the residual crosstalk, clearly illustrating the reduced noise boost caused by $\mathrm{PR}_{1.1.b}$. Eye diagrams at the slicer input are a commonly used metric in high-speed links for comparison purposes. Fig. 9 shows the received slicer input eye diagrams at 10 Gb/s using PR_1, $\mathrm{PR}_{1.1}$, and $\mathrm{PR}_{1.1.b}$. The variable optimized tap, b_{opt}, is canceled by a 1-tap DFE in $\mathrm{PR}_{1.1.b}$. As seen in the figure, $\mathrm{PR}_{1.1.b}$ has a larger eye opening when compared with PR_1 and $\mathrm{PR}_{1.1}$ equalizations at 10 Gb/s. Increasing the speed while keeping the number of TX PR equalizer taps unchanged leads to more residual ISI in PR_1 equalization, which can further reduce the RX eye opening, as explained in Section II. Fig. 10 shows the receiver eye diagram for the $\mathrm{PR}_{1.1.b}$ at 15 Gb/s. As seen in the figure, while PR_1 equalization results in a completely closed eye at the receiver, $\mathrm{PR}_{1.1.b}$ outperforms $\mathrm{PR}_{1.1}$ (duobinary) equalization. The eye diagram results show the potential improvements offered by PR equalization in current and future links at higher data rates. The improvements provided by PR equalizers is expected to be more pronounced at higher speeds and more dense interconnects. A summary of the link simulations for the different equalization strategies is shown in Table II for a typical 12-in channel with connectors. At 10 Gb/s, $\mathrm{PR}_{1.1.b}$ resulted in a 49% and 28% larger eye height and a 10% larger width when compared with PR_1 and $\mathrm{PR}_{1.1}$ equalizations, respectively. At 15 Gb/s, PR_1 equalization has a completely closed eye. However, in comparison with $\mathrm{PR}_{1.1}$, $\mathrm{PR}_{1.1.b}$ increases the eye height by 19% and the eye width by 7%. These promising results combined with its suitability for high-speed and low-complexity implementation shows that $\mathrm{PR}_{1.1.b}$ is an excellent candidate for future high-speed multichannel links.

TABLE II
PERFORMANCE SUMMARY FOR 12-in MICROSTRIP WITH CONNECTORS

PR	*Eye-H(mV) 10Gb/s*	*Eye-W(UI) 10Gb/s*	*Eye-H(mV) 15Gb/s*	*Eye-W(UI) 15Gb/s*
1	72.5	0.56	0	0
11	84.6	0.56	35.7	0.44
11b	108.2	0.62	42.7	0.47

VII. CONCLUSION

The benefits of PR equalization and the impact on crosstalk has been presented in this paper. The proposed receiver architecture for $\mathrm{PR}_{1.1.b}$ relaxes the loop timing issue, allowing for a speed increase of nearly two times compared with traditional DFE receiver implementations in the same technology with little or no impact on the complexity. An MMSE optimization problem was developed and PR equalizer performance was compared for some typical channels. Our simulation results, based on measured channel responses, indicate that the receiver architecture with a target PR of $[1\ 1\ b]$ outperforms both full channel (PR_1) and duobinary $(\mathrm{PR}_{1.1})$ equalizations for a wide range of channels. PR equalization is a promising candidate for high-speed links which can potentially reduce the crosstalk noise, while increasing the receiver eye opening.

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